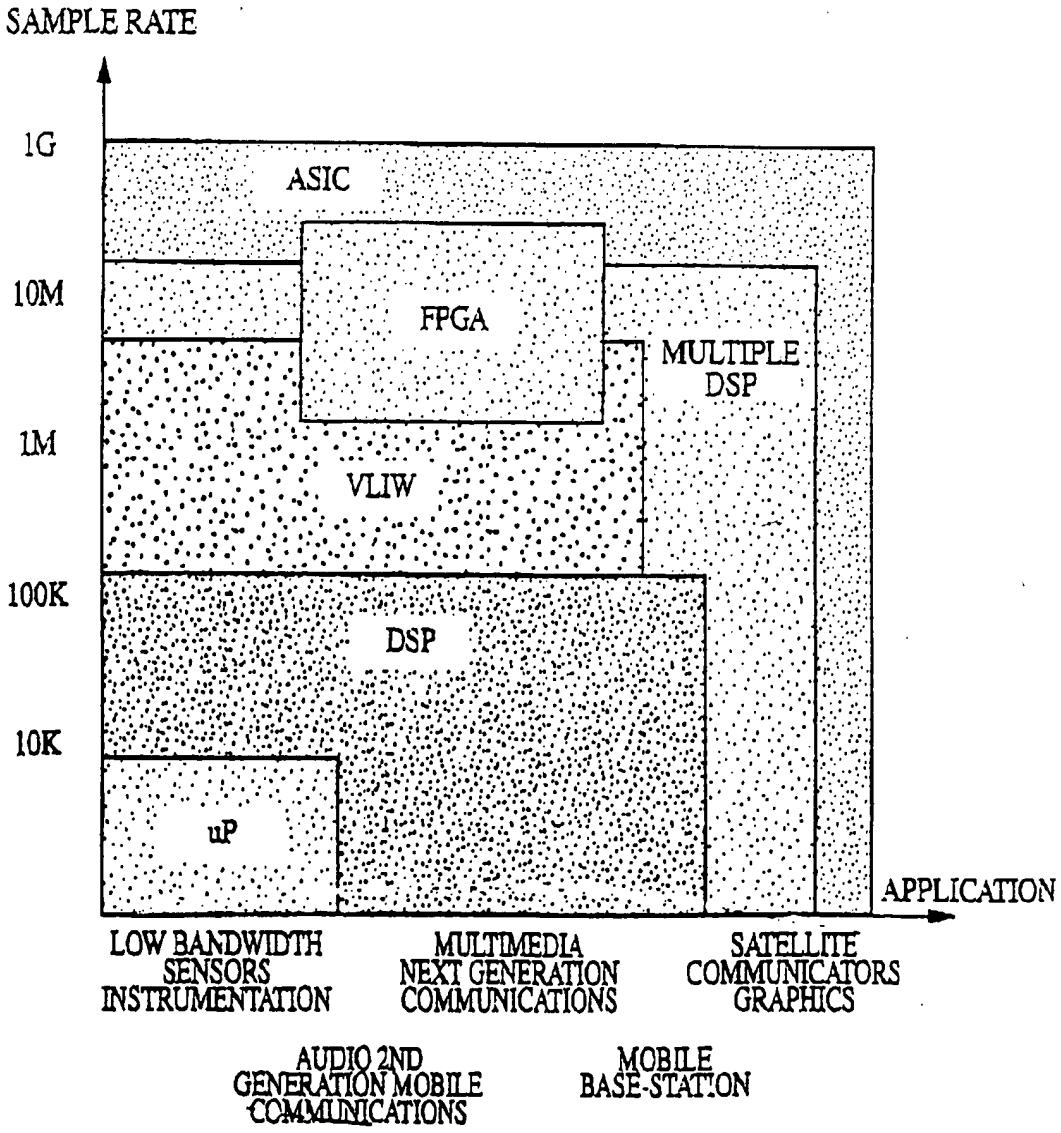

SAMPLE RATE
1G
10M
1M
100K
10K
ASIC
FPGA
MULTIPLE DSP
VLIW
DSP
uP
APPLICATION
LOW BANDWIDTH SENSORS INSTRUMENTATION
AUDIO 2ND GENERATION MOBILE COMMUNICATIONS
MULTIMEDIA NEXT GENERATION COMMUNICATIONS
MOBILE BASE-STATION
SATELLITE COMMUNICATORS GRAPHICS

FIG. 1

FIG. 2

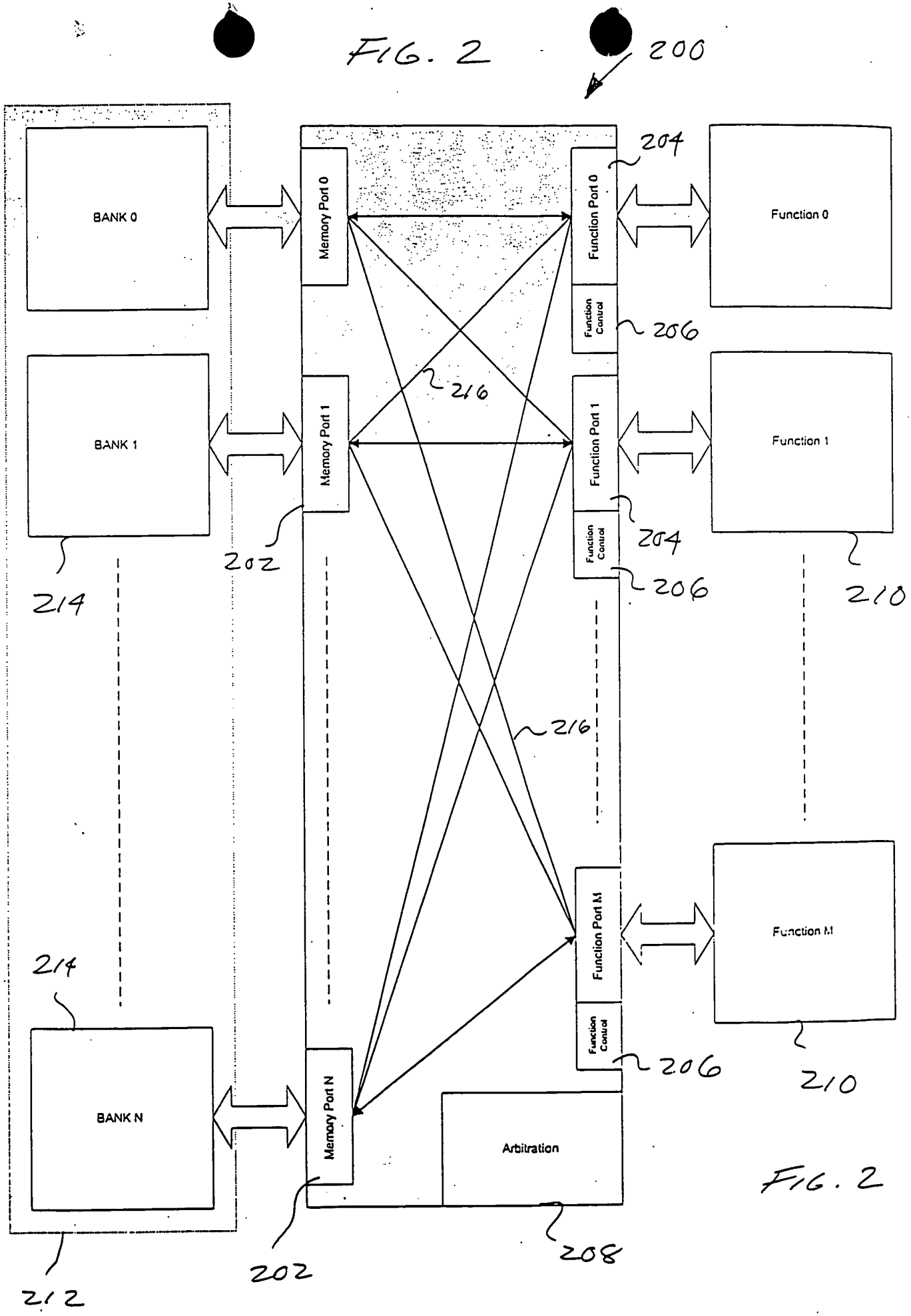

200
BANK 0
BANK 1
BANK N
Memory Port 0
Memory Port 1
Memory Port N
Function Port 0
Function Port 1
Function Port M
Function Control
Function 0
Function 1
Function M
Arbitration
204
206
216
214
202
210
212
208

FIG. 2

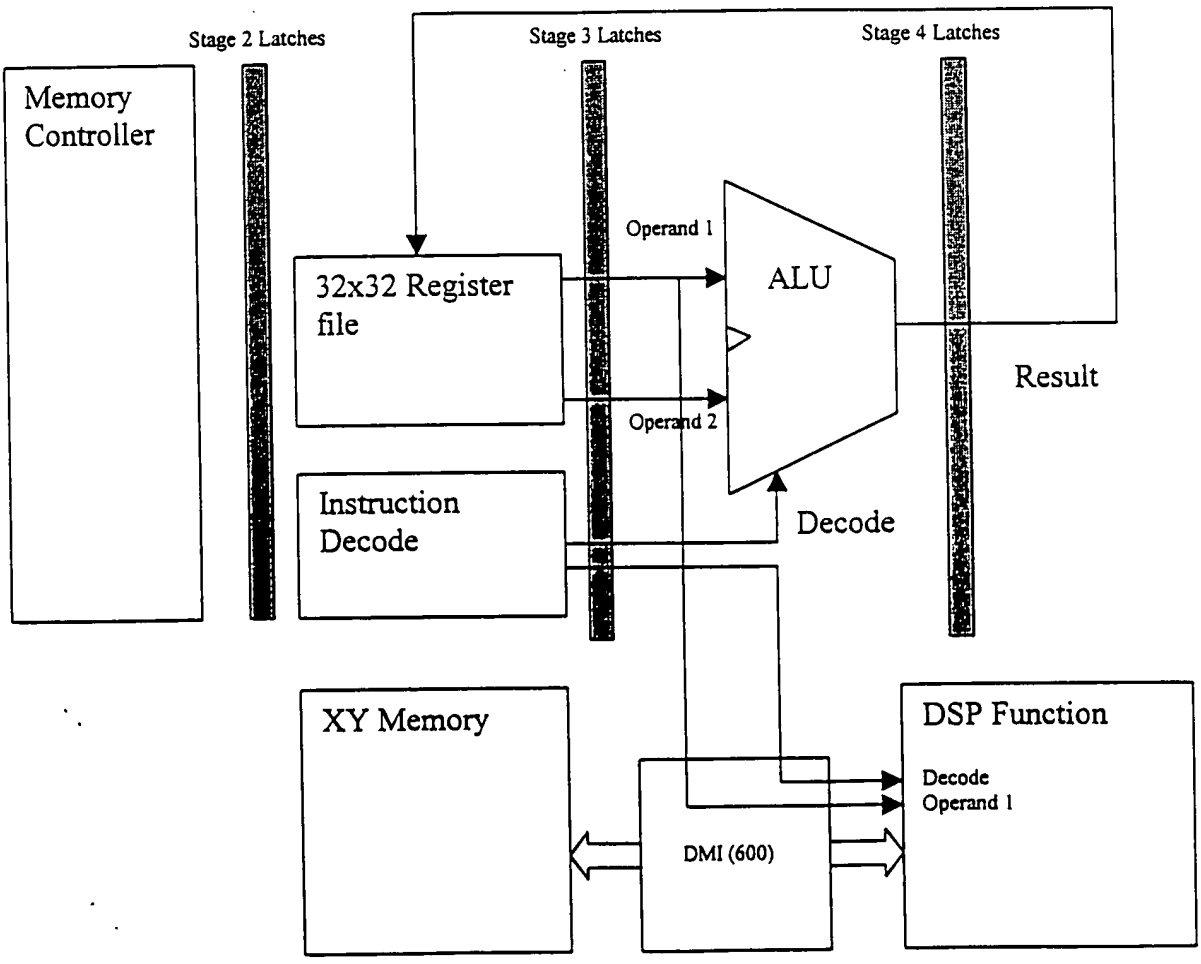

Stage 2 Latches
Stage 3 Latches
Stage 4 Latches
Memory Controller
32x32 Register file
Operand 1
Operand 2
ALU
Result
Instruction Decode
Decode
XY Memory
DMI (600)
DSP Function
Decode
Operand 1

Fig. 2a

FIG. 3

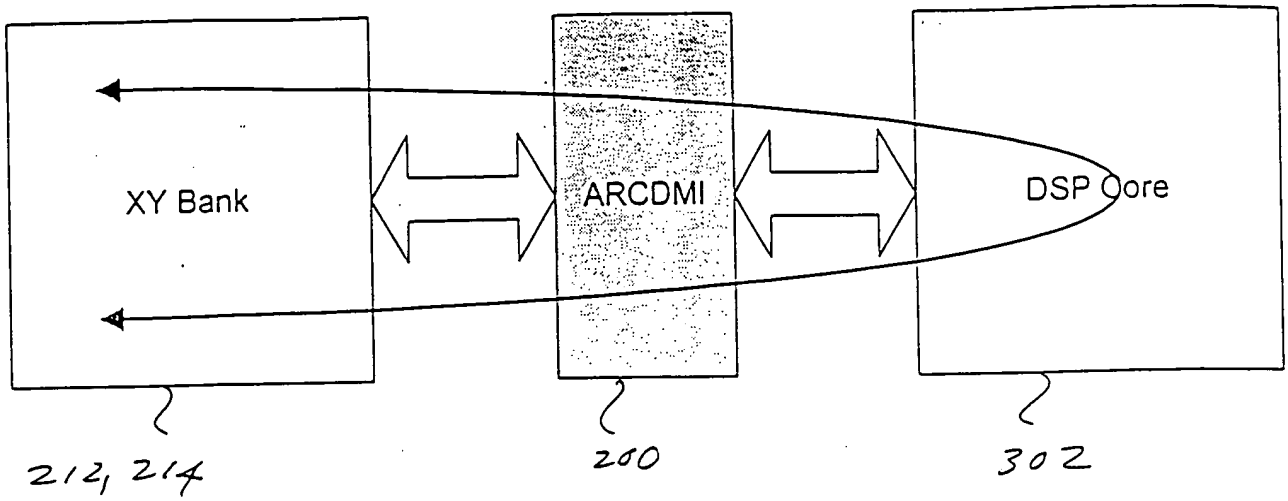

XY Bank
ARCDMI
DSP Core
212, 214
200
302

FIG. 5

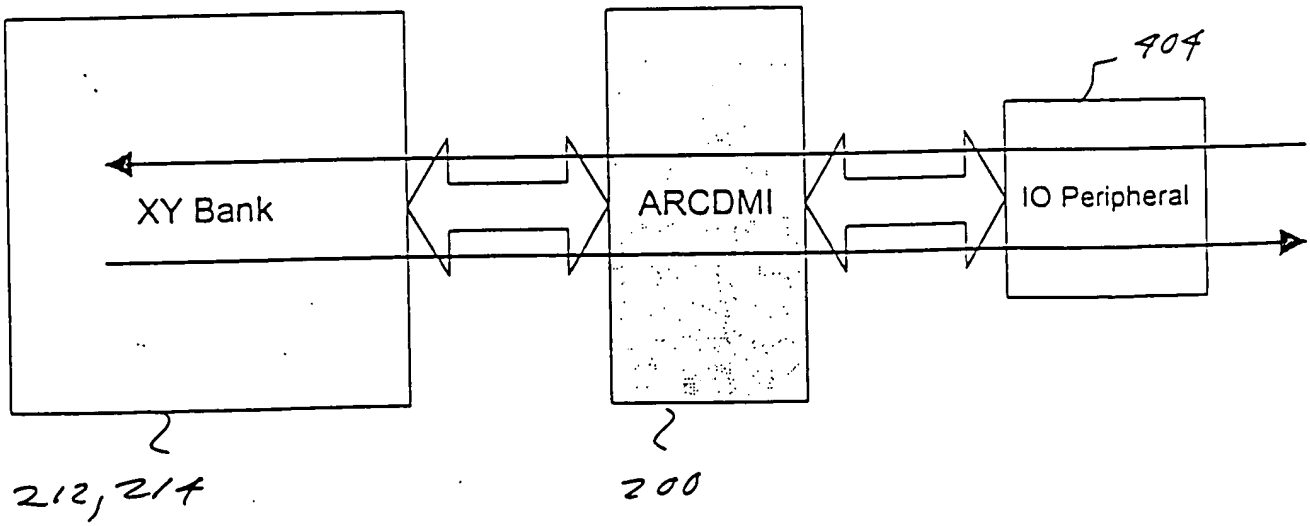
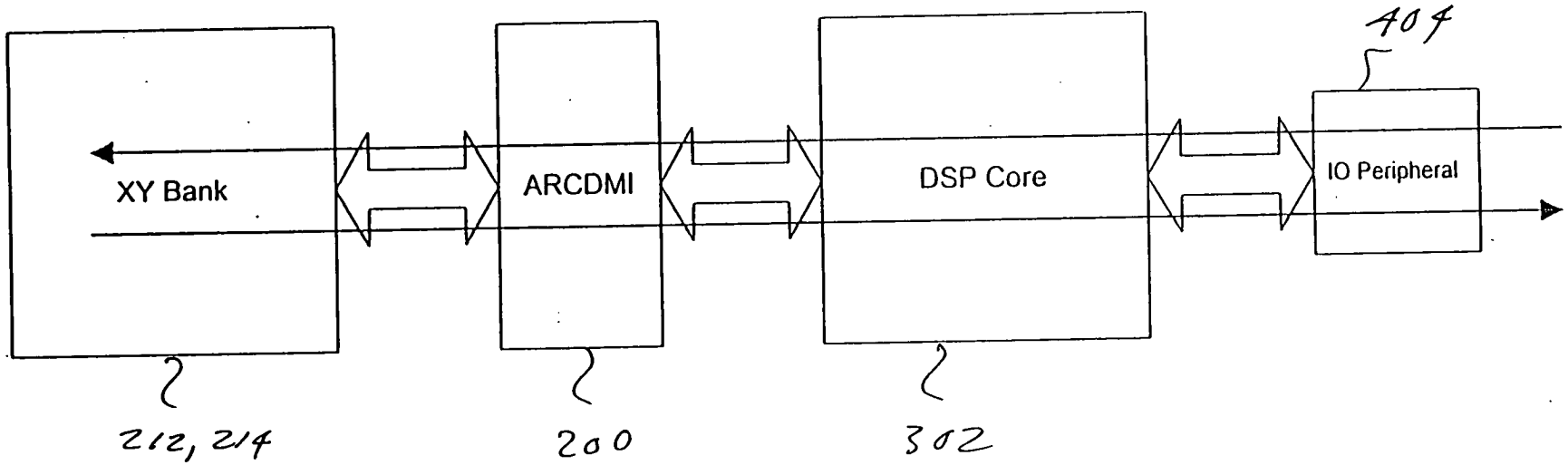

404
XY Bank
ARCDMI
IO Peripheral
212, 214
200

FIG. 4



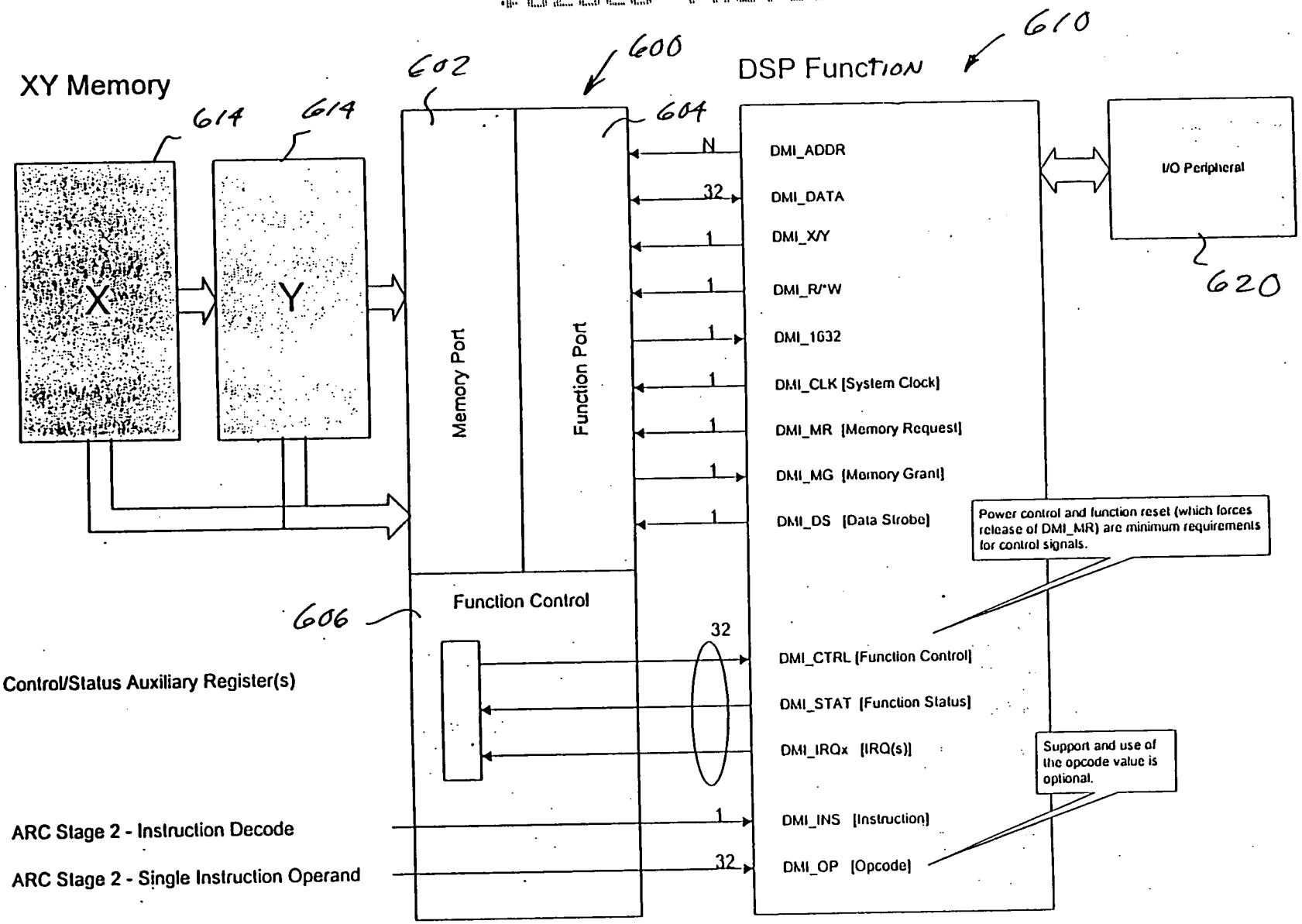

XY Memory
602
600
610
DSP Function
614
614
604
X
Y
Memory Port
Function Port
N
32
1
1
1
1
1
1
1
DMI_ADDR
DMI_DATA
DMI_X/Y
DMI_R/*W
DMI_1632
DMI_CLK [System Clock]
DMI_MR [Memory Request]
DMI_MG [Memory Grant]
DMI_DS [Data Strobe]
I/O Peripheral
620
Power control and function reset (which forces release of DMI_MR) are minimum requirements for control signals.
606
Function Control
32
DMI_CTRL [Function Control]
DMI_STAT [Function Status]
DMI_IRQx [IRQ(s)]
Control/Status Auxiliary Register(s)
Support and use of the opcode value is optional.
1
32
DMI_INS [Instruction]
DMI_OP [Opcode]
ARC Stage 2 - Instruction Decode
ARC Stage 2 - Single Instruction Operand

Fig. 6

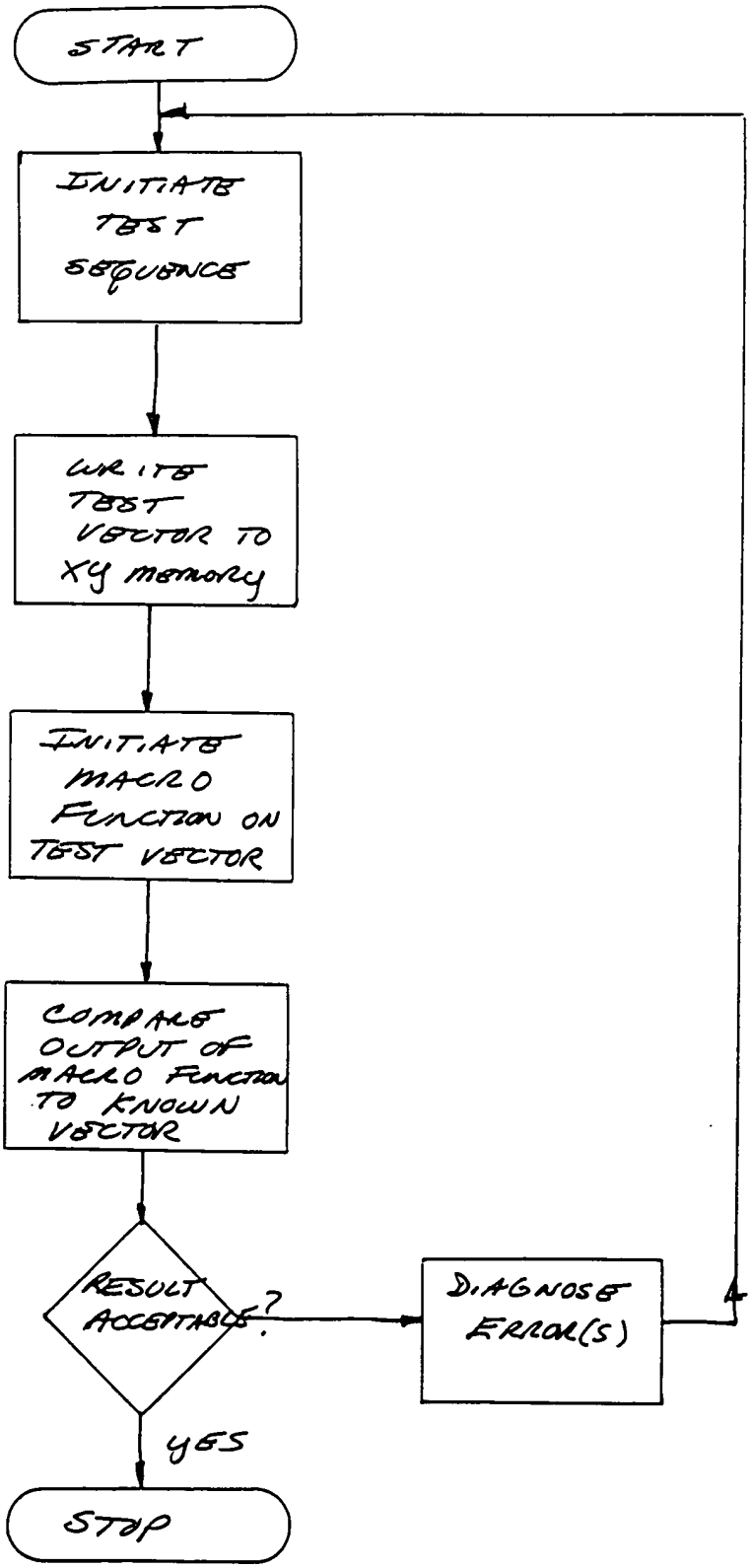
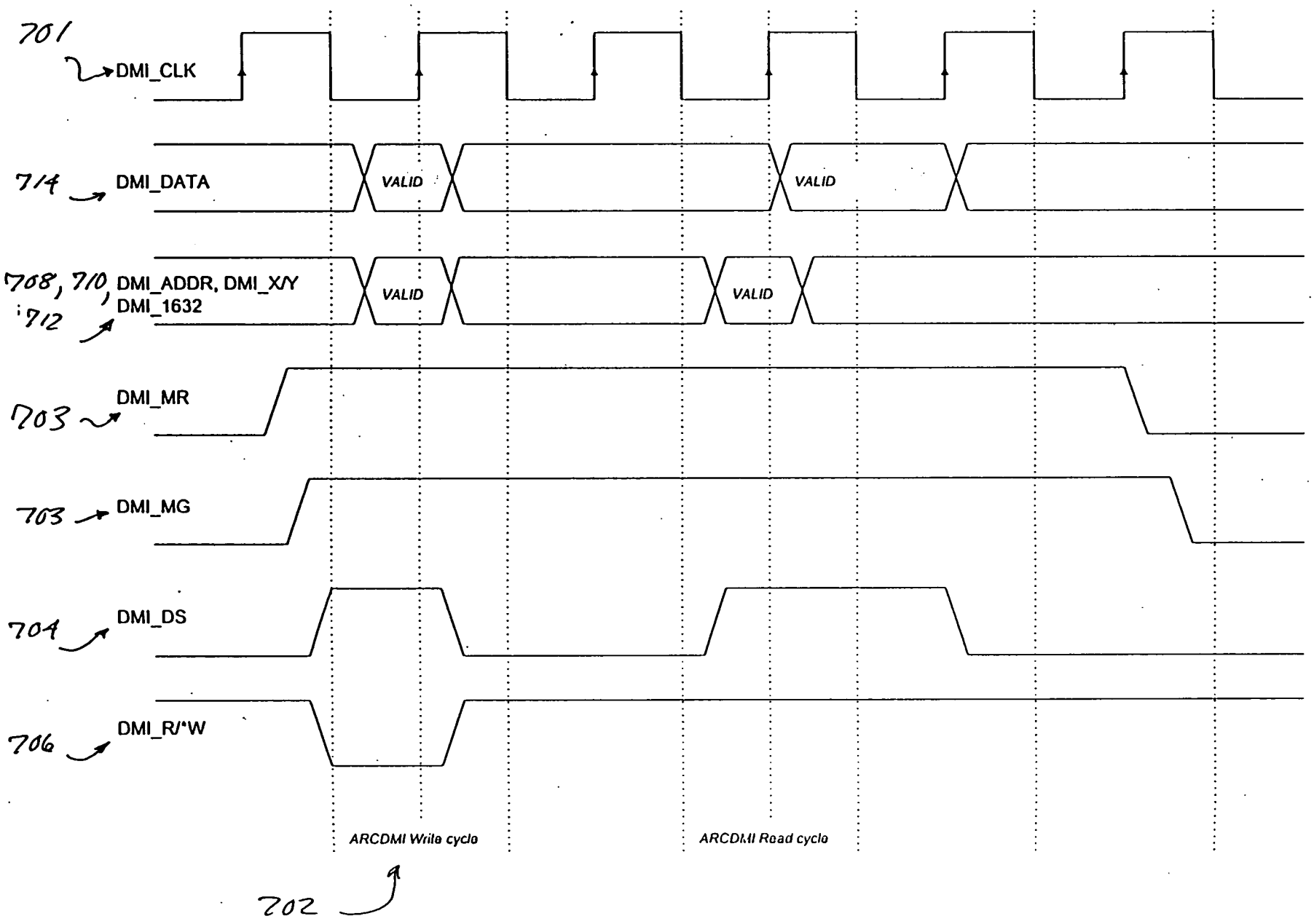

START
INITIATE TEST SEQUENCE
WRITE TEST VECTOR TO XY MEMORY
INITIATE MACRO FUNCTION ON TEST VECTOR
COMPARE OUTPUT OF MACRO FUNCTION TO KNOWN VECTOR
RESULT ACCEPTABLE?
DIAGNOSE ERROR(S)
YES
STOP

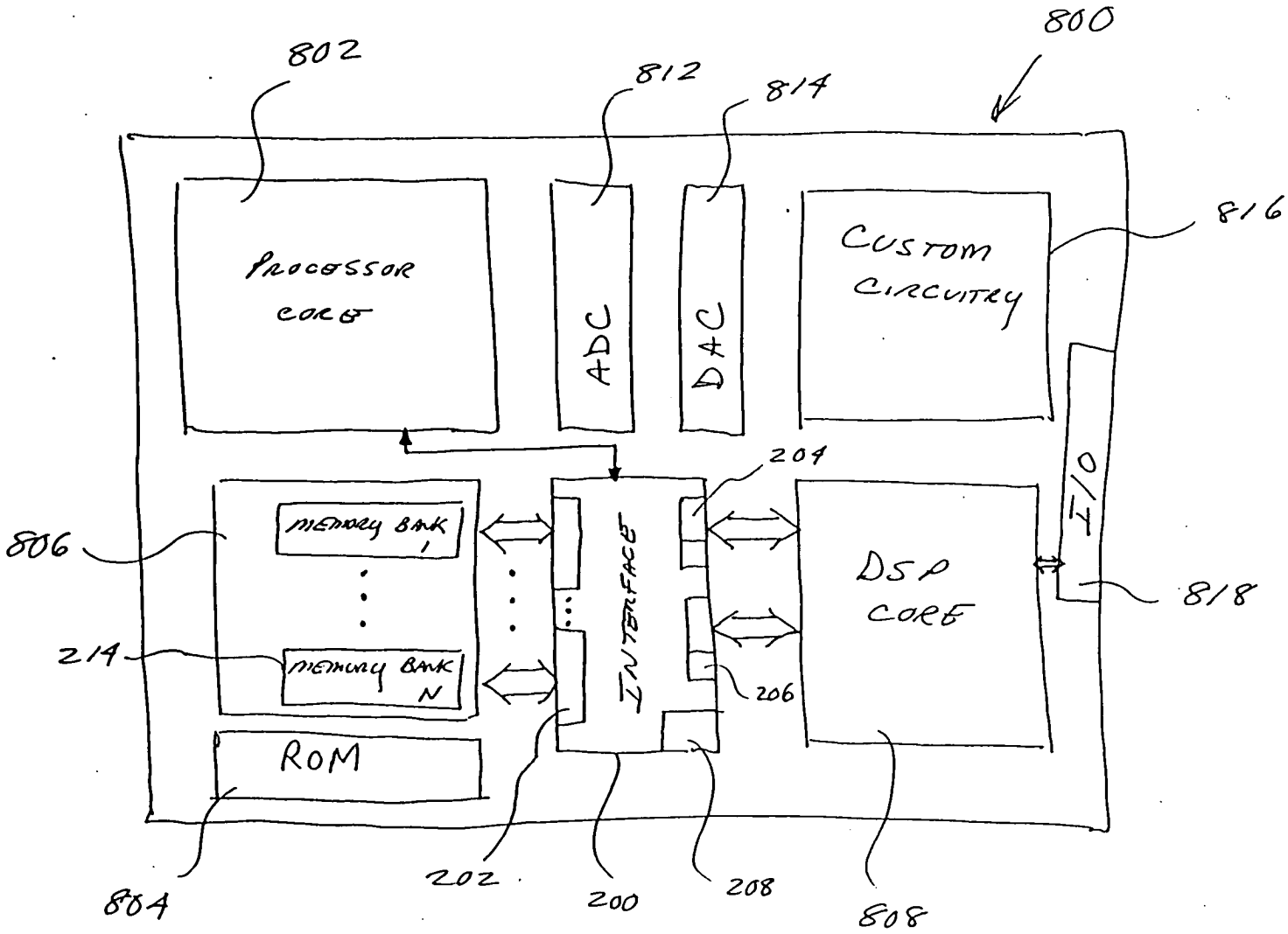
FIG. 6a

FIG. 7


701
DMI_CLK
714
DMI_DATA
VALID
VALID
708, 710, 712
DMI_ADDR, DMI_X/Y
DMI_1632
VALID
VALID
703
DMI_MR
703
DMI_MG
704
DMI_DS
706
DMI_R/*W
ARCDMI Write cycle
ARCDMI Read cycle
702

TO2060" TH2T0860

FIG. 8



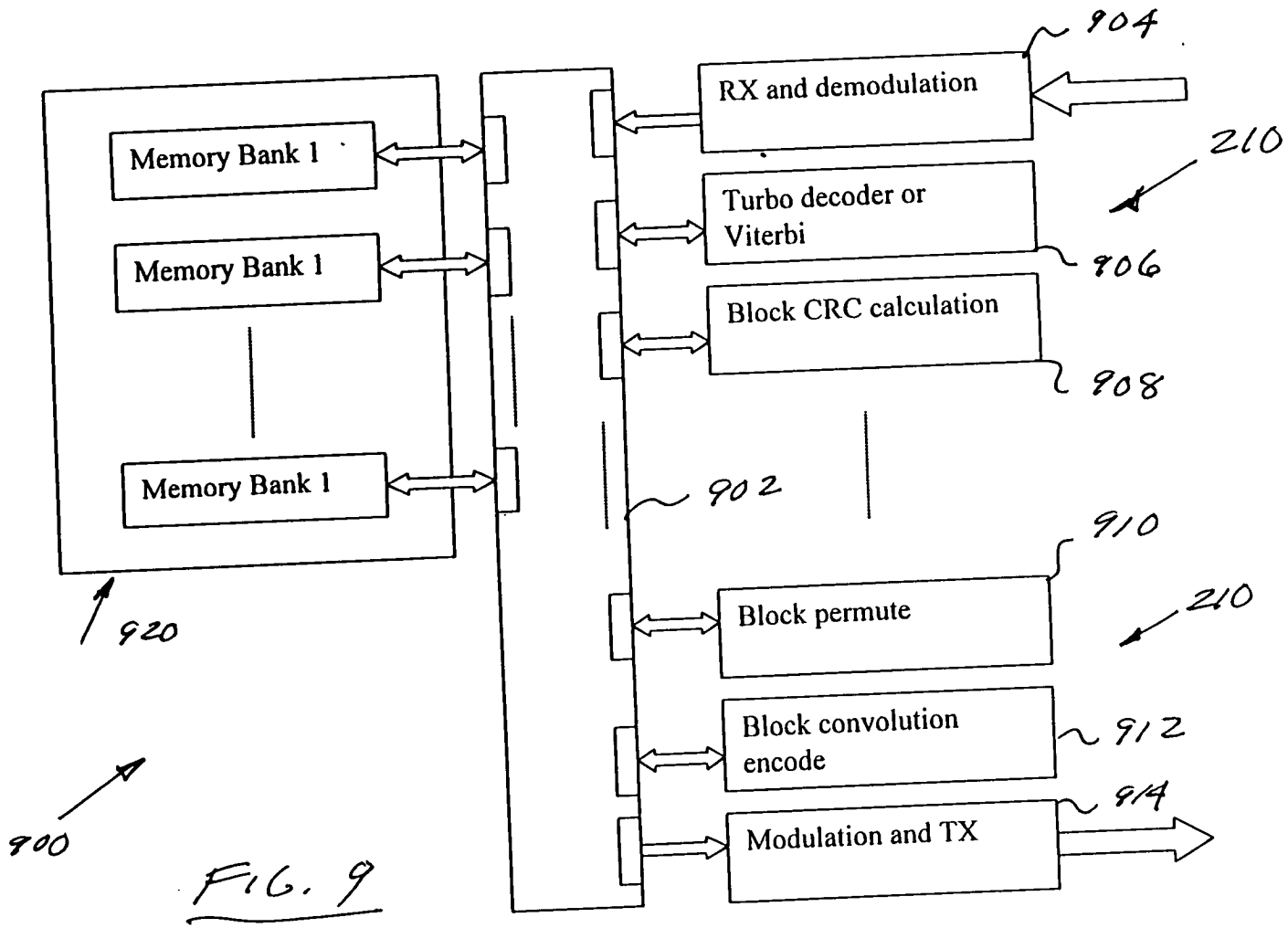

Memory Bank 1
Memory Bank 1
Memory Bank 1
920
900
RX and demodulation
904
210
Turbo decoder or Viterbi
906
Block CRC calculation
908
902
910
Block permute
210
Block convolution encode
912
Modulation and TX
914

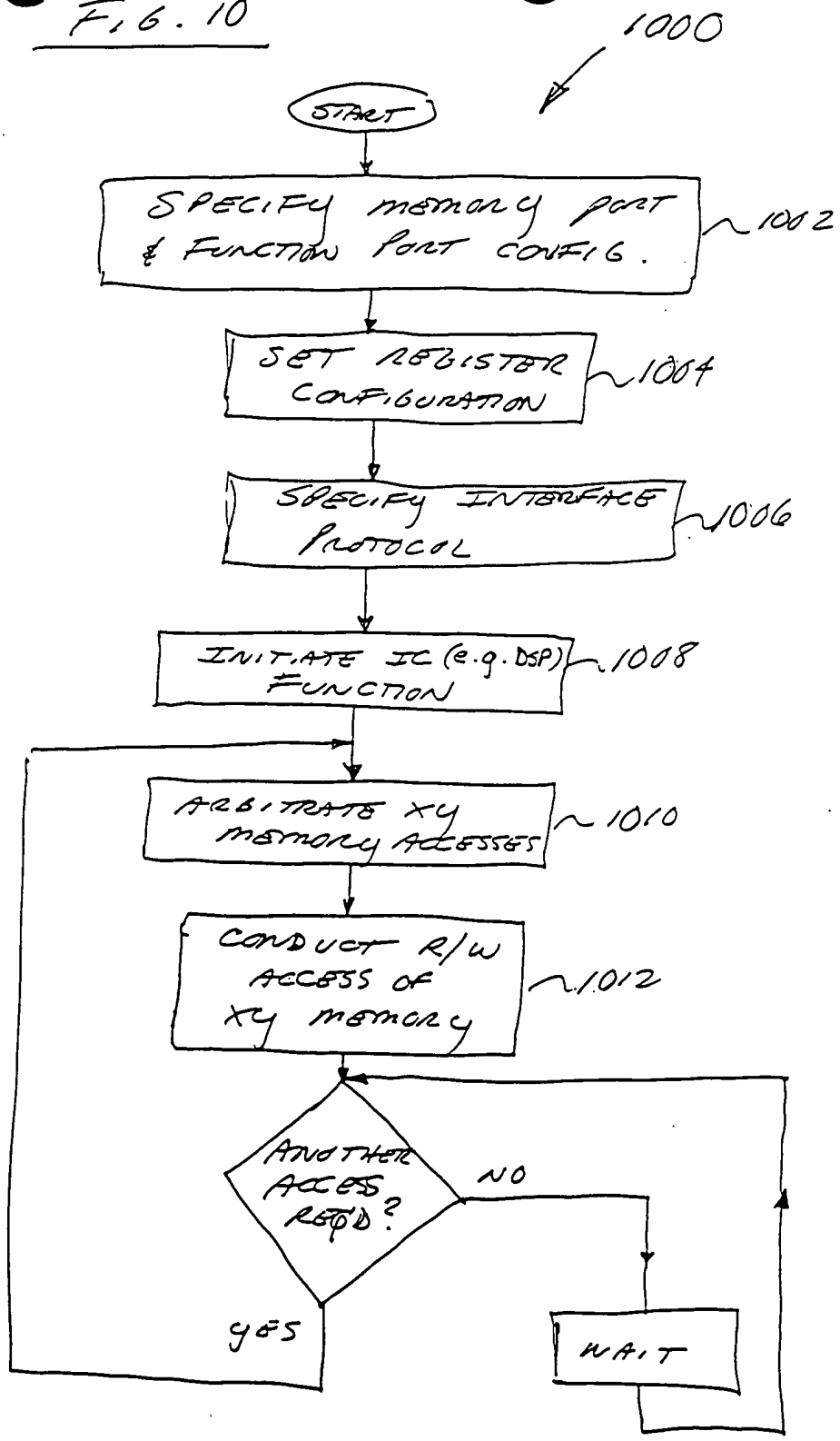
FIG. 9

	Data Block 0	Data Block 1	Data Block 2	Data Block 3	Data Block 4	...
Bank 0	Function 0	Function 1	Function 2	Function 3	Function 0	
Bank 1	-	Function 0	Function 1	Function 2	Function 3	
Bank 2	-	-	Function 0	Function 1	Function 2	
Bank 3	-	-	-	Function 0	Function 1	

FIG. 9a

1042050 "14/12/2050

FIG. 10


1000
START
SPECIFY MEMORY PORT & FUNCTION PORT CONFIG.
1002
SET REGISTER CONFIGURATION
1004
SPECIFY INTERFACE PROTOCOL
1006
INITIATE IC (e.g. DSP) FUNCTION
1008
ARBITRATE XY MEMORY ACCESSES
1010
CONDUCT R/W ACCESS OF XY MEMORY
1012
ANOTHER ACCESS REQ'D?
NO
YES
WAIT

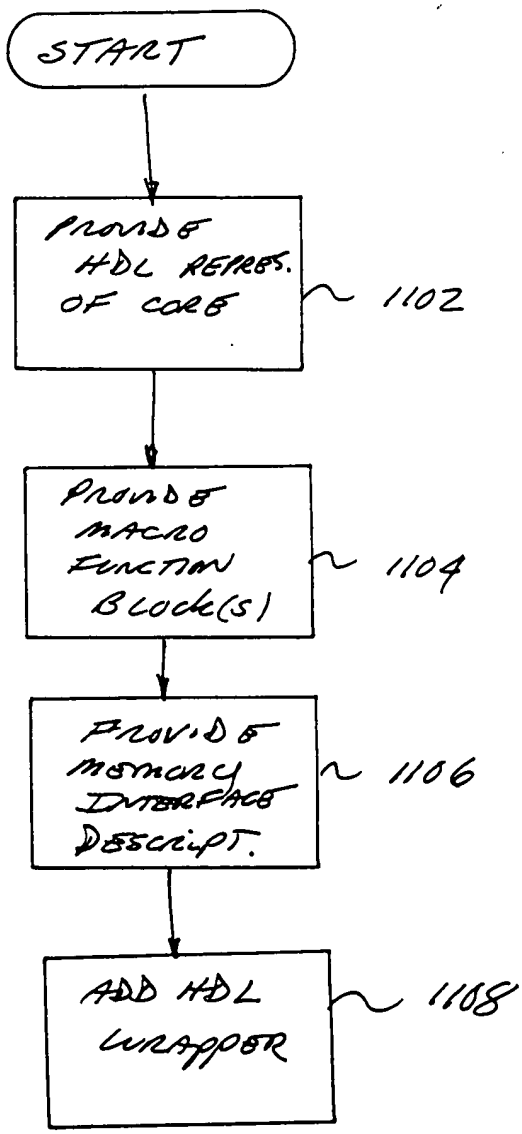

START
1100
PROVIDE HDL REPRES. OF CORE
1102
PROVIDE MACRO FUNCTION BLOCK(S)
1104
PROVIDE MEMORY INTERFACE DESCRIPT.
1106
ADD HDL WRAPPER
1108

FIG. 11

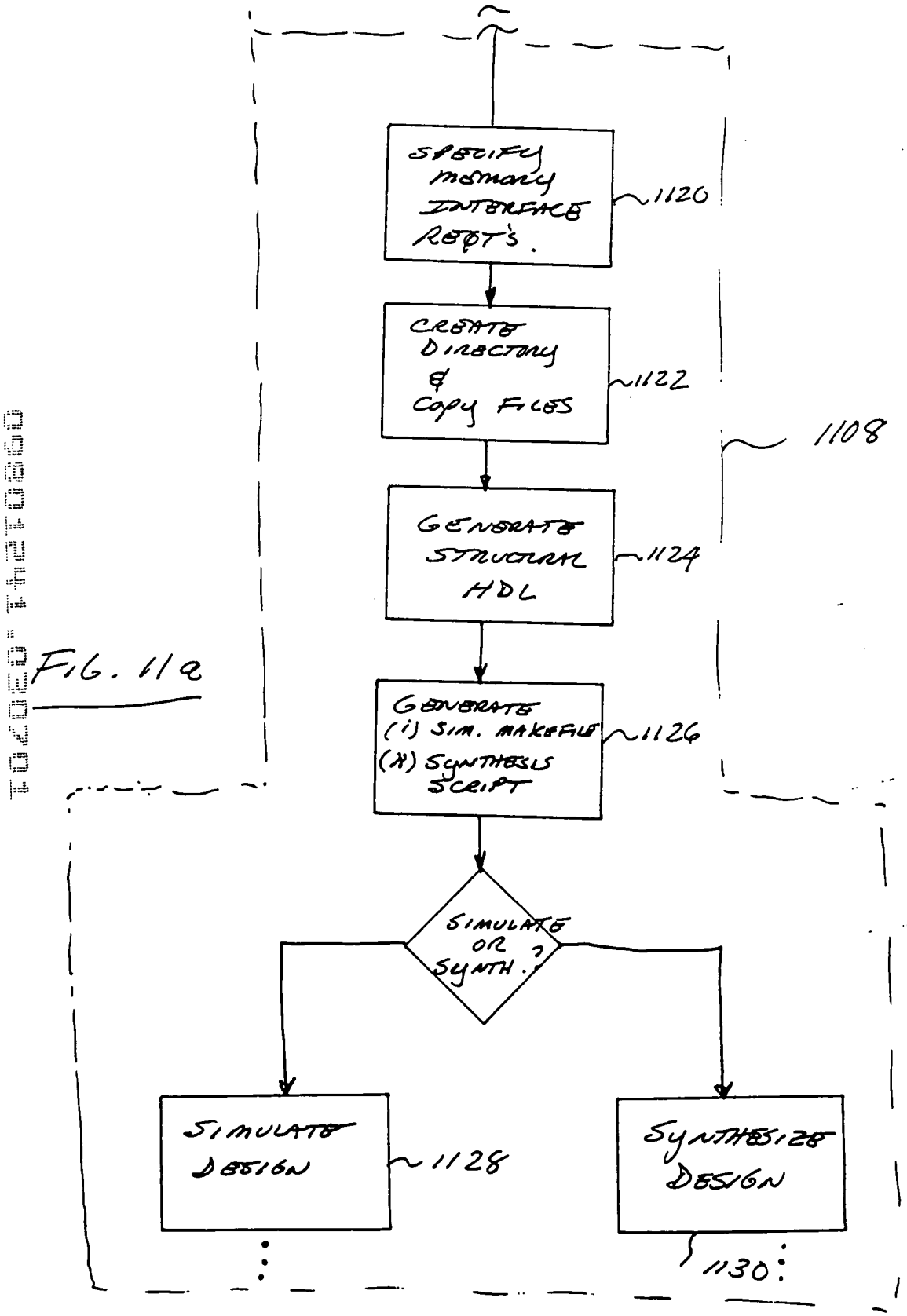
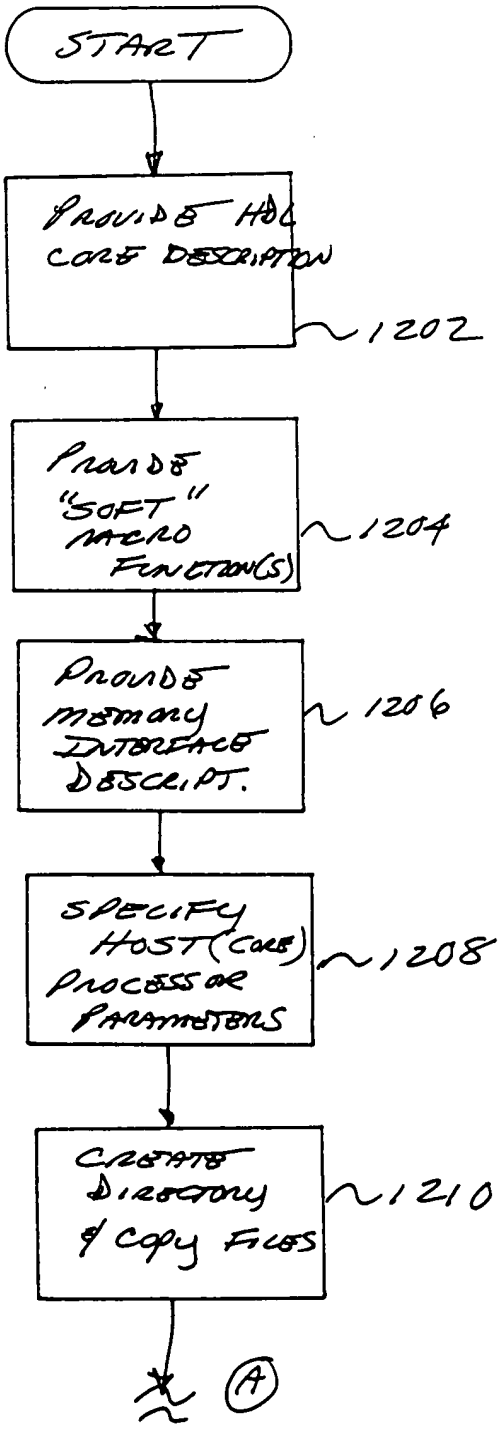

SPECIFY MEMORY INTERFACE REPT's.
1120
CREATE DIRECTORY & COPY FILES
1122
1108
GENERATE STRUCTURAL HDL
1124
GENERATE (i) SIM. MAKEFILE (ii) SYNTHESIS SCRIPT
1126
SIMULATE OR SYNTH.?
SIMULATE DESIGN
1128
SYNTHESIZE DESIGN
1130

FIG. 11a

TOKEN-THIEF

FIG. 12
(PART 1 OF 2)



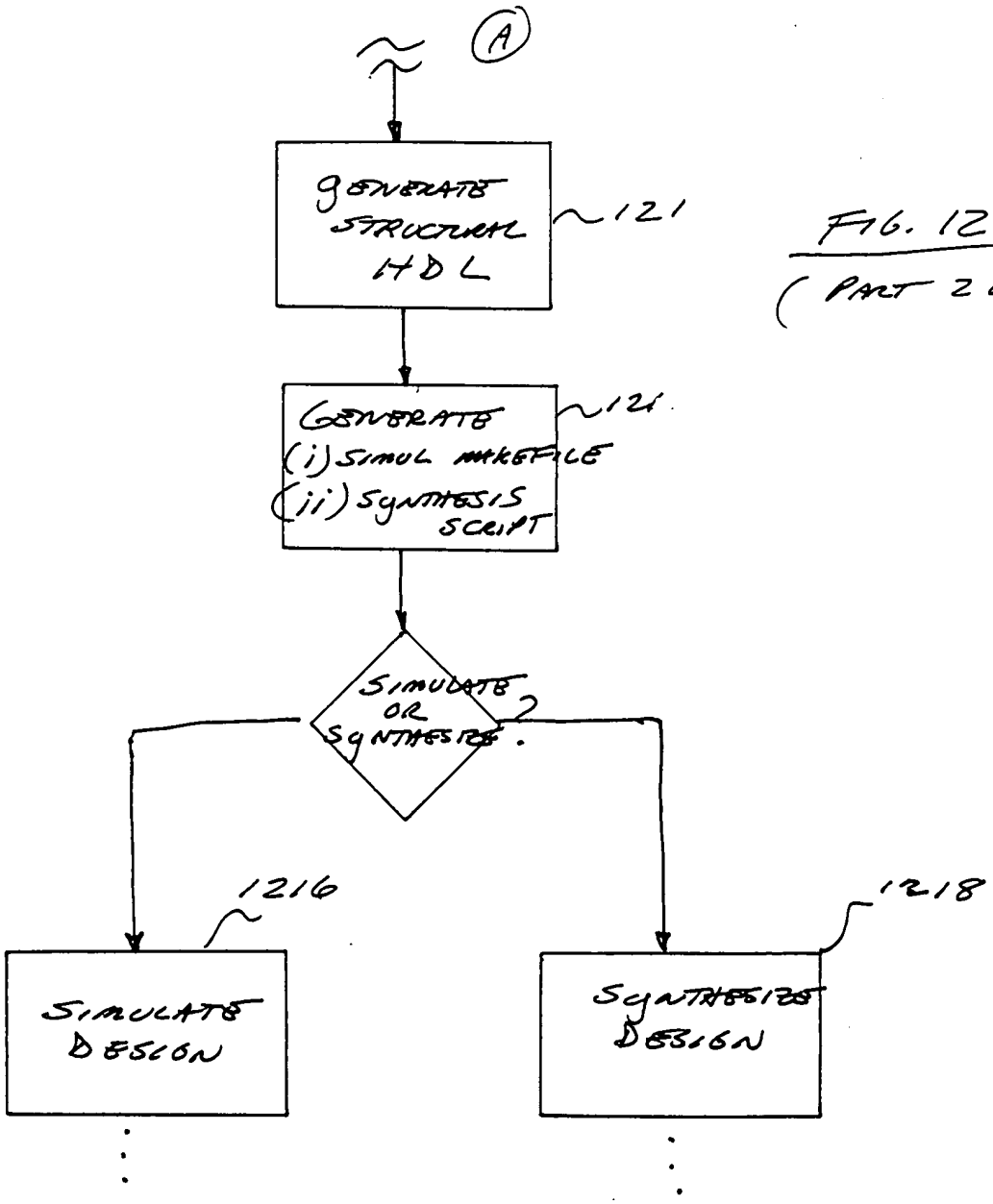


FIG. 12
(PART 2 OF 2)